AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A device to synthesize a range of frequencies F1-F2 with high spectral purity, comprising:

a variable-step synthesizer having a division rank Na providing a range of frequencies F3-F4;

a variable ratio divider having a division factor Nb connected to said variable step-synthesizer for receiving the range of frequencies from said variable-step synthesizer; and

a frequency control device adapted for delivering a division rank command of [[a]] the variable ratio divider, a command of the frequency of said variable-step synthesizer, and a command of a synthesis step of said variable-step synthesizer and connected at one output to said variable-step frequency synthesizer and at another output to said variable ratio divider,

wherein a length of [[the]] a cycle of evolution of the division rank Na is variable and dependent on [[the]] a value of the division factor Nb, and said variable-step synthesizer is a fractional step phase-locked loop synthesizer using a constant frequency step ΔF which is a fraction of a reference frequency Fref and the reference frequency Fref is chosen so that ~~the desired fractional step values are obtained as follows~~:

- Fref is a function of a sequence of [[the]] values N1, N2, … Np that may be assumed by Nb where the sequence of the values N1, N2 … Np either follows an arithmetic or non-arithmetic progression, and
- Fref/ΔF must be a multiple of the least common multiple of N1, N2, … Np ~~where ΔF is a constant frequency step~~.

2. (Previously Presented) The device according to claim 1 comprising a filtering device positioned after the variable ratio divider Nb.

3. (Canceled).

4. (Previously Presented) The device according to claim 1 wherein the variable ratio divider Nb is a value from N1 to Np, the values N1 to Np follow an arithmetic progression, and wherein a maximum frequency of the synthesizer is given by F4=N1*F2 where N1 is the smallest value of the sequence of values N1 to Np and the frequency F3 is a function of N2.

5. (Original) The device according to claim 4 wherein the value of the frequency F3 is substantially equal to or slightly lower than (N1/N2)*F4.

6. (Previously Presented) The device according to claim 1 wherein the variable ratio divider Nb is a value from N1 to Np, the values N1 to Np following a non-arithmetic progression.

7. (Previously Presented) The device according to claim 6 wherein F3 is substantially equal to or smaller than a F4 where a is the smallest value obtained in dividing two consecutive values one after the other.

8. (Original) The device according to claim 6 wherein the highest division rank Nb is chosen.

9. (Previously Presented) The device according to claim 1 further comprising a mixer receiving an output signal from the variable step synthesizer and a mixing signal.

10. (Currently Amended) A method of synthesizing a range of frequencies F1-F2 with high spectral purity a frequency source which comprises the steps of:

dividing an output signal of a voltage controlled oscillator by a first value Nb, and [[;]]

dividing an input signal of the voltage controlled <u>oscillator</u> by a second value Na,

wherein a length of a cycle of evolution of Na is variable and dependent on a value of Nb.

11. (Previously Presented) The method according to claim 10 wherein a value of Nb varies according to an arithmetic sequence N1...Np and wherein a frequency F4 is determined by N1*F2 and a frequency F3 is a function of N2.

12. (Previously Presented) The method according to claim 11 wherein a value of the frequency F3 is chosen to be substantially equal to or slightly below (N1/N2)*F4.

13. (Previously Presented) The method according to claim 10 wherein a value of Nb varies according to a non-arithmetic sequence and wherein two consecutive values of the sequence are divided.

14. (Previously Presented) The method according to claim 13 wherein F3 is substantially equal to or smaller than a F4 where a is the smallest value obtained in dividing two consecutive values of the sequence.

15. (Original) The method according to claim 14 wherein the highest division rank Nb is chosen.

16. (Previously Presented) The method according to claim 10, wherein the modification of the division rank and the synthesis step is simultaneous.

17. (Previously Presented) The method according to claim 1, wherein a ratio of a reference frequency to the frequency step, is a least common multiple of the sequence N1...Np.

18. (Previously Presented) The device according to claim 1 wherein reference frequency Fref is chosen so that the desired fractional step values are obtained.

19. (Previously Presented) The method according to claim 10 wherein the reference frequency Fref is chosen so that the desired fractional step values are obtained as Fref is a function of sequence of the values N1, N2, … Np assumed by Nb.

20. (Previously Presented) The method according to claim 10 wherein the reference frequency Fref is chosen so that the desired fractional step values are obtained as follows Fref/ΔF must be a multiple of the LCM of N1, N2, … Np with ΔF a given frequency step.